REMARKS

Claims 1-6 and 24-29 were presented for examination. Claims 1-6 and 24-29 have been rejected under 35 U.S.C. § 103(a). The following comments address all stated grounds for rejection, and place the presently pending claims, as identified above, in condition for allowance.

I. Claims 1-6 Rejected Under 35 U.S.C. § 103(a)

Claims 1-6 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,854,801 to Yamada et al. (Yamada). Applicants respectfully traverse this rejection and contend that Yamada does not detract from the patentability of claims 1-6.

Claim 1 provides a test generator in an integrated circuit coupled to a memory array to generate a physical address in the memory array and to generate a test vector for the physical address. Further, claim 1 provides a conversion circuit in the integrated circuit to convert the physical address in the memory array to a logical address in the memory array to allow the test vector to be written to the logical address of the memory.

Yamada discusses an improvement of conventional semiconductor test systems for testing memory of a semiconductor device. Yamada provides a test pattern generator; an address wrap conversion circuit; and an address inversion scramble to improve the prior art semiconductor test system. The address inversion scramble of Yamada is used to convert a logical address from the pattern generator and address wrap conversion circuit to a physical address of the device under test. Yamada provides the address inversion scramble function to convert the address in cases where the physical address internal to the device does not match the logical address that is external to the device. The wrap conversion circuit is provided with data Y0-Y8 corresponding to the bit length of the column address and data Z0-Z2 corresponding to the bit length of the wrap address, Y0-Y2, of the SDRAM. The logic structure of the wrap conversion circuit converts the data Y0-Y2 by logically combining it with Z0-Z2, as shown in Figures 3 and 4 of Yamada. The main purpose of the wrap conversion circuit is to allow the wrap address Y0-Y2 to be controlled by Z0-Z2, according to a simple logic equation, to generate sequential type or interleave type addresses, rather then using a complex pattern program produced by a mathematical process.

Yamada fails to teach or suggest a conversion circuit in an integrated circuit to convert a physical address in the memory array to a logical address in the memory array to allow the test vector to be written to the logical address of the memory. In contrast to the claimed invention, Yamada provides converting a logical address that is external to the device to a physical address in a memory array internal to the device. That is, the inversion scramble of Yamada converts the logical address provided by the pattern generator to a physical address of the device for cases where the physical address that is internal to the device does not match the logical address that is external to the device. The conversion circuit of the present invention is distinguished from the inversion scramble of Yamada, because the present invention requires converting from a physical address in the memory array to a logical address in the memory array and Yamada teaches converting from an external logical address to an internal physical address of the device. As such, neither the wrap conversion circuit nor the inversion scramble teach or suggest a conversion circuit that converts a physical address to a logical address.

Further, Yamada fails to teach or suggest a test generator in an integrated circuit coupled to a memory array to generate a physical address in a memory array and to generate a test vector for the physical address. Yamada provides a pattern generator that generates a logical address. The inversion scramble of Yamada converts the logical address provided by the pattern generator to a physical address of the device for cases where the physical memory alignment internal to the device does not match the logical address external to the device. The test generator of the present invention is distinguished from the pattern generator of Yamada, because the test generator of the present invention generates a physical address in the memory array, while the pattern generator of Yamada generates a logical address.

Furthermore, Yamada does not teach or suggest the integrated circuit of Claim 1. *In re Larson* 340 F.2d 965, 144 USPQ 347 (CCPA 1965) does not support a conclusion that the single structure of Claim 1 is merely an engineering choice and not patentable. *In re Larson* concerns a mechanical assembly having a unitary construction recited in U.S. patent application serial No. 7282 as opposed to the prior art mechanical assembly, which included several parts rigidly secured together as a single unit. The Court held the prior art assembly comprising several parts rigidly secured together as a single unit were so combined as to constitute a unitary whole and hence the use of a one-piece construction versus a multi-piece construction of the mechanical

assembly was a matter of an engineering design choice. No such replication of an assembly so combined with fasteners and later formed without fasteners is recited in Claim 1. That is, the separate and distinct components of Yamada are not so combined as to constitute a unitary whole structure. Yamada teach or suggest that the pattern generator, wrap conversion circuit, inversion scramble and memory devices comprise an assembly that is rigidly secured together as a single unit. In further distinction, the test system of Yamada is developed to be reused to test many SDRAM devices, not a single SDRAM device as the claimed invention requires. That is, the claimed invention is concerned with built in self testing of a device and provides a single integrated circuit that includes memory and circuitry necessary for testing the memory. One skilled in the art would not be motivated to combine separate and distinct components of Yamada into a single integrated circuit as the Applicants have claimed, because Yamada does not teach a unitary structure for built in self test, but rather provides separate and distinct components for a test system to provide mass testing of memory devices.

Additionally, the claimed invention has the structure, the function and the operability to perform neighborhood pattern sensitive testing. In contrast, the system taught by Yamada has a structure, function and operation that is different from the invention of Claim 1, and therefore is not capable of performing neighborhood pattern sensitive testing. The conversion from a physical address in the memory array to a logical address in the memory array of the claimed invention allows the claimed invention to perform neighborhood pattern sensitive testing using built-in self test. Neighborhood sensitive testing requires generating sequences of physical addresses for memory cells that are physically adjacent, but not necessarily sequentially addressed. This allows the claimed invention to exercise each physical address of memory cells surrounding the memory cell of the physical address under test, and allows detection of any interaction between the physical address under test and the surrounding adjacent physical addresses. By contrast, Yamada is concerned with generating the sequential type address for testing of the physical addresses of a device by generating a sequential logical addresses and converting the sequential logical addresses to match the sequential physical addresses for a sequential type address SDRAM device.

For at least these reasons, Applicants respectfully contend that Yamada does not teach or suggest all of the patentable features of claim 1. Claims 2-6 depend on claim 1, and therefore

incorporate all of the patentable features of claim 1. Applicants respectfully request the Examiner to reconsider and withdraw the rejection of claims 1-6 under 35 U.S.C. § 103(a).

II. Claims 24-29 Rejected Under 35 U.S.C. § 103(a)

Claims 24-29 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamada. Applicants respectfully traverse this rejection and contend that Yamada does not detract from the patentability of claims 24-29.

Claim 24 provides a conversion circuit in a semiconductor device, coupled to a test circuit wherein the test circuit provides a physical memory row address for a selected group of memory cells under test to the conversion circuit for conversion of the provided physical memory address to a logical memory address for the selected group of memory cells under test.

Yamada fails to teach or suggest a conversion circuit in a semiconductor device for conversion of the provided physical memory address to a logical memory address. In contrast to the claimed invention, Yamada provides converting a logical address that is external to the device to a physical address in a memory array internal to the device. That is, the inversion scramble of Yamada converts the logical address provided by the pattern generator to a physical address of the device for cases where the physical address that is internal to the device does not match the logical address that is external to the device. The claimed invention requires converting from a physical memory address to a logical memory address, while Yamada teaches converting from a logical address to a physical address of the device. As such, Yamada fails to teach or suggest a conversion circuit that converts a physical address to a logical address.

Further, Yamada fails to teach or suggest a test circuit that provides a physical memory row address for a selected group of memory cells under test to the conversion circuit. Yamada provides a pattern generator that generates a logical address. The inversion scramble of Yamada converts the logical address provided by the pattern generator to a physical address of the device for cases where the physical memory alignment internal to the device does not match the logical address external to the device. The test circuit of the present invention is distinguished from the pattern generator of Yamada, because the test circuit of the present invention generates a physical address, while the pattern generator of Yamada generates a logical address.

Furthermore, Yamada does not teach or suggest the semiconductor device of Claim 24. *In re Larson* 340 F.2d 965, 144 USPQ 347 (CCPA 1965) does not support a conclusion that the single structure of Claim 24 is merely an engineering choice and not patentable. *In re Larson* concerns a mechanical assembly having a unitary construction recited in U.S. patent application serial No. 7282 as opposed to the prior art mechanical assembly, which included several parts rigidly secured together as a single unit. The Court held the prior art assembly comprising several parts rigidly secured together as a single unit were so combined as to constitute a unitary whole and hence the use of a one-piece construction versus a multi-piece construction of the mechanical assembly was a matter of an engineering design choice. No such replication of an assembly so combined with fasteners and later formed without fasteners is recited in Claim 1. That is, the separate and distinct components of Yamada are not so combined as to constitute a unitary whole structure. Yamada teach or suggest that the pattern generator, wrap conversion circuit, inversion scramble and memory devices comprise an assembly that is rigidly secured together as a single unit. In further distinction, the test system of Yamada is developed to be reused to test many SDRAM devices, not a single SDRAM device as the claimed invention requires. That is, the claimed invention is concerned with built in self testing of a device and provides a single semiconductor device that includes memory and circuitry necessary for testing the memory. One skilled in the art would not be motivated to combine separate and distinct components of Yamada into a semiconductor device as the Applicants have claimed, because Yamada does not teach a unitary structure for built in self test, but rather provides separate and distinct components for a test system to provide mass testing of memory devices.

Additionally, the claimed invention has the structure, the function and the operability to perform neighborhood pattern sensitive testing. In contrast, the system taught by Yamada has a structure, function and operation that is different from the invention of Claim 1, and therefore is not capable of performing neighborhood pattern sensitive testing. The conversion from a physical address in the memory array to a logical address in the memory array of the claimed invention allows the claimed invention to perform neighborhood pattern sensitive testing using built-in self test. Neighborhood sensitive testing requires generating sequences of physical addresses for memory cells that are physically adjacent, but not necessarily sequentially addressed. This allows the claimed invention to exercise each physical address of memory cells surrounding the memory cell of the physical address under test, and allows detection of any

interaction between the physical address under test and the surrounding adjacent physical addresses. By contrast, Yamada is concerned with generating the sequential type address for testing of the physical addresses of a device by generating a sequential logical addresses and converting the sequential logical addresses to match the sequential physical addresses for a sequential type address SDRAM device.

For at least these reasons, Applicants respectfully contend that Yamada does not teach or suggest all of the patentable features of claim 24. Claims 25-29 depend on claim 24, and therefore incorporate all the patentable features of claim 24. Applicants respectfully request the Examiner to reconsider and withdraw the rejection of claims 24-29 under 35 U.S.C. § 103(a).

Application No.: 09/835170 Docket No.: SMQ-041RCE/P5213

III. Conclusion

In view of the above remarks, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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